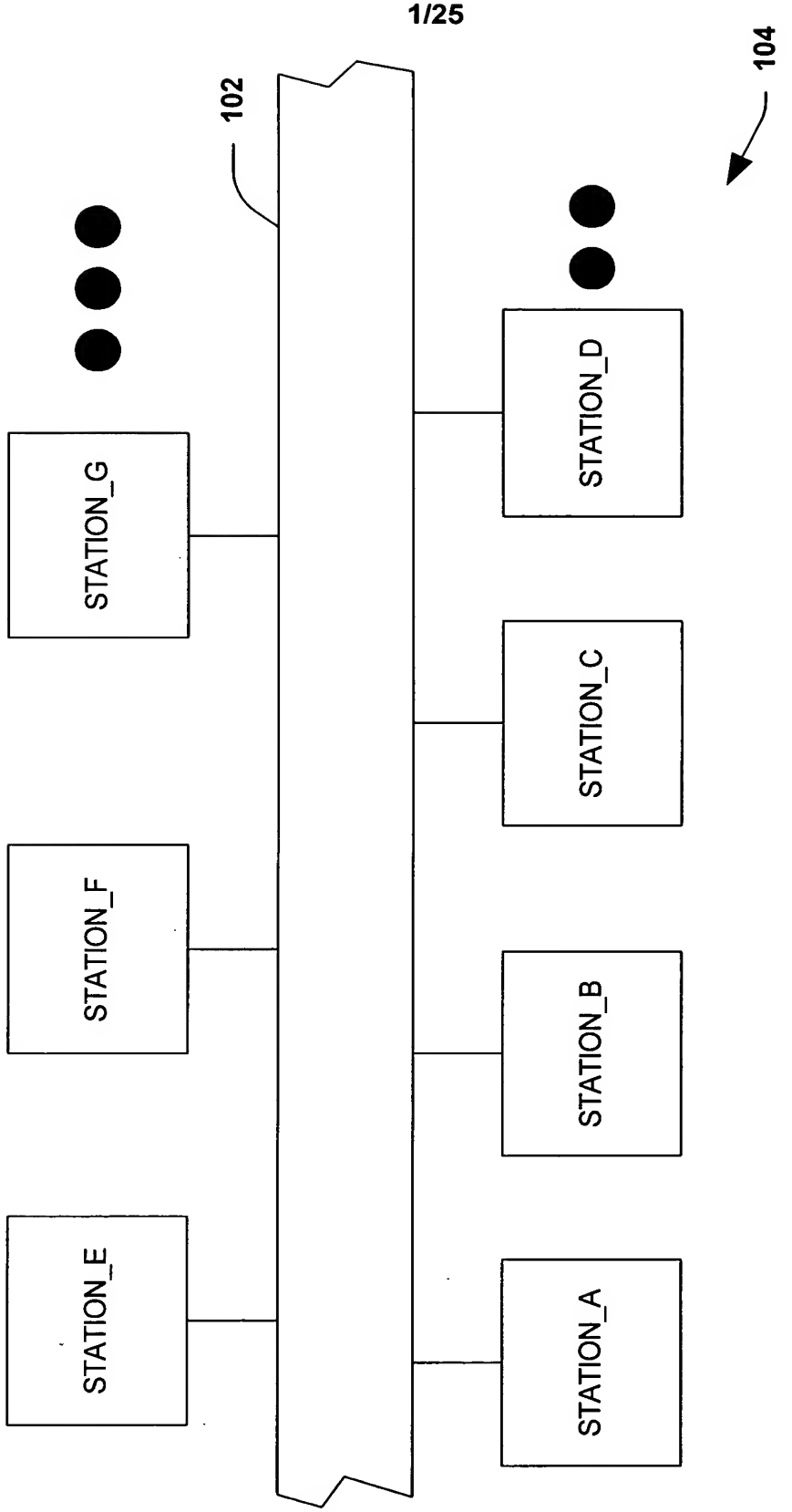
102
104
STATION_G
STATION_F
STATION_E
STATION_D
STATION_C
STATION_B
STATION_A
100

FIG. 1

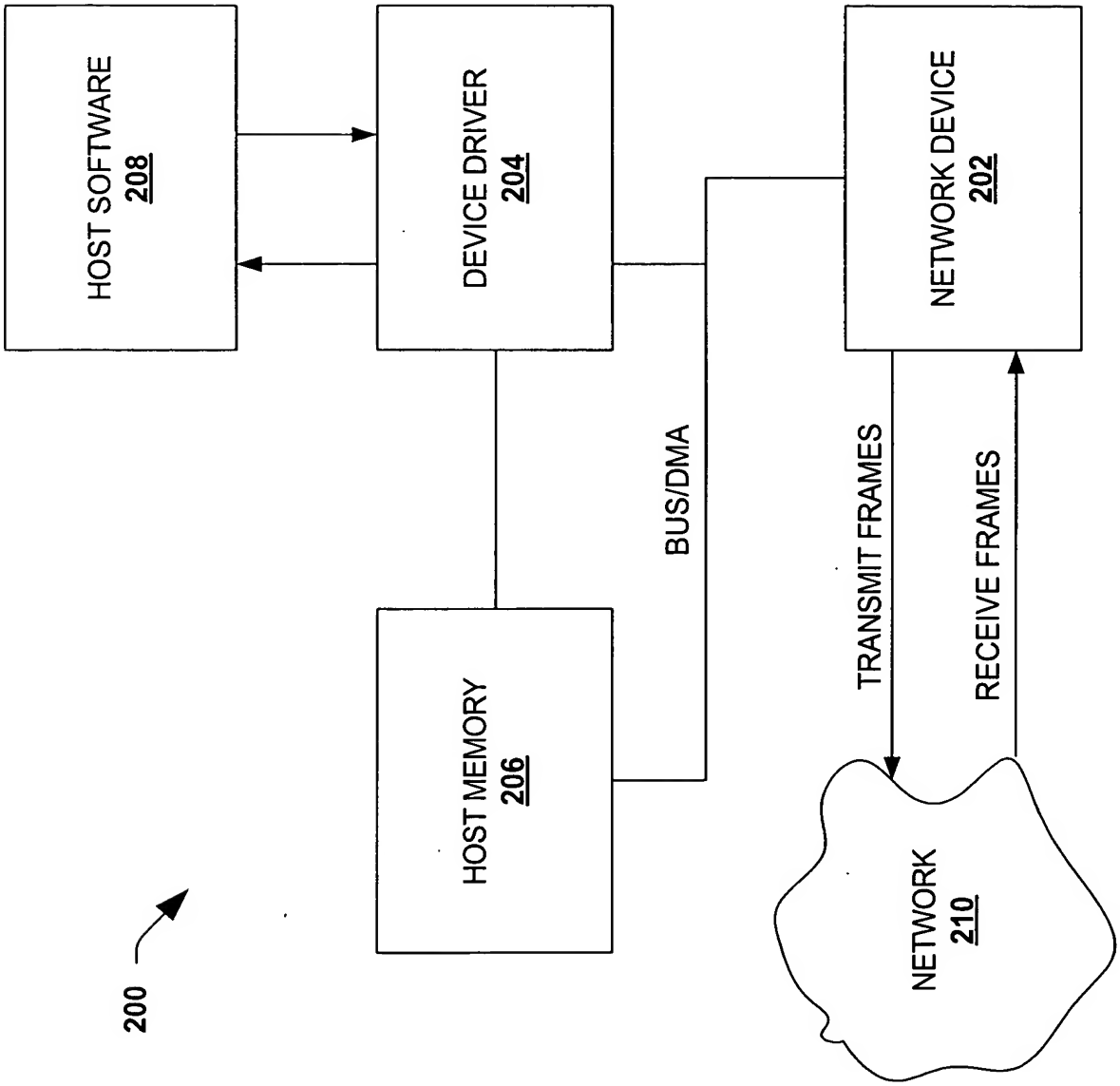
HOST SOFTWARE
208
DEVICE DRIVER
204
NETWORK DEVICE
202
HOST MEMORY
206
BUS/DMA
TRANSMIT FRAMES
RECEIVE FRAMES
NETWORK
210
200

FIG. 2

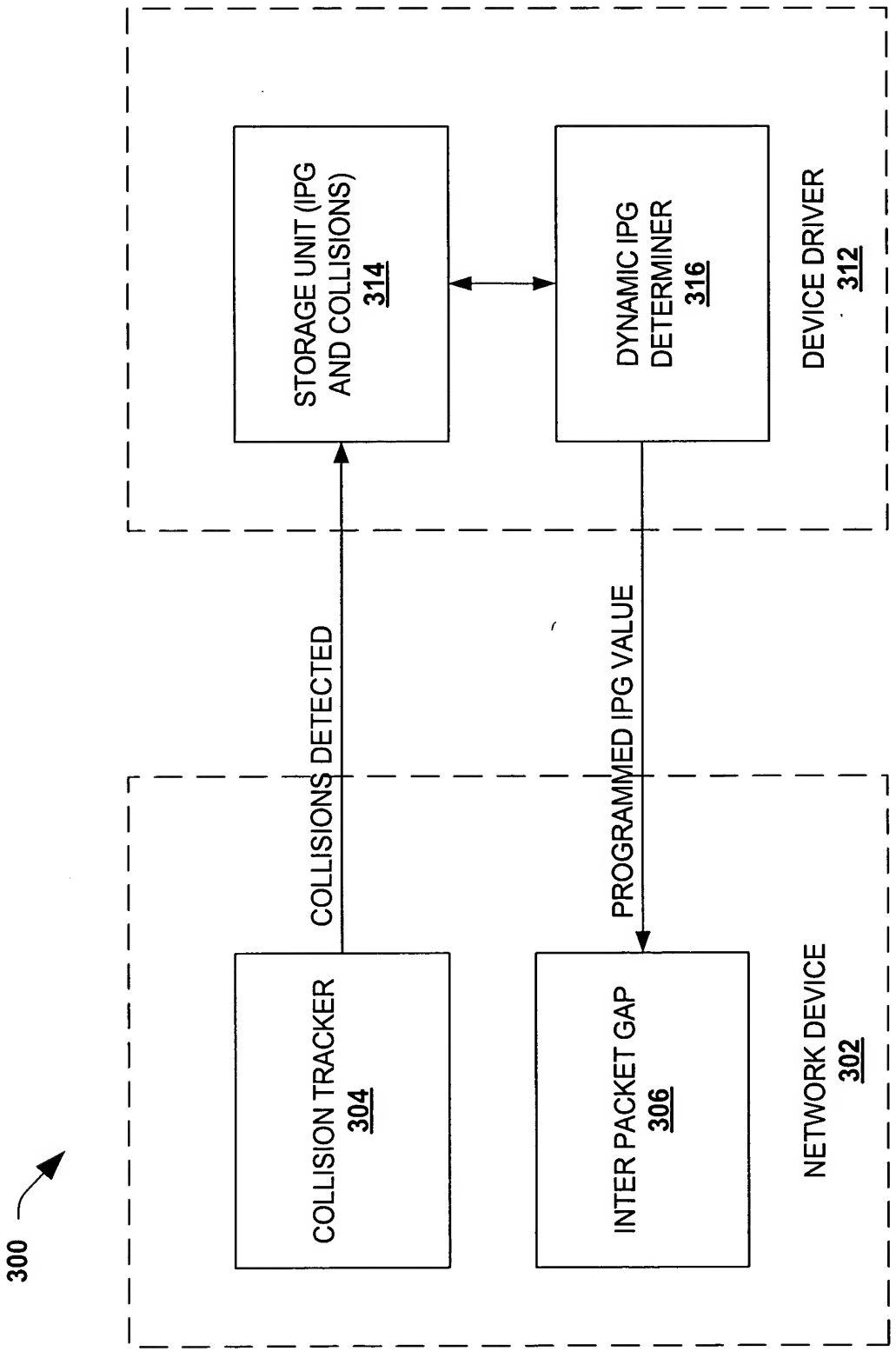
300
NETWORK DEVICE
302
COLLISION TRACKER
304
INTER PACKET GAP
306
COLLISIONS DETECTED
PROGRAMMED IPG VALUE
DEVICE DRIVER
312
STORAGE UNIT (IPG AND COLLISIONS)
314
DYNAMIC IPG DETERMINER
316

FIG. 3

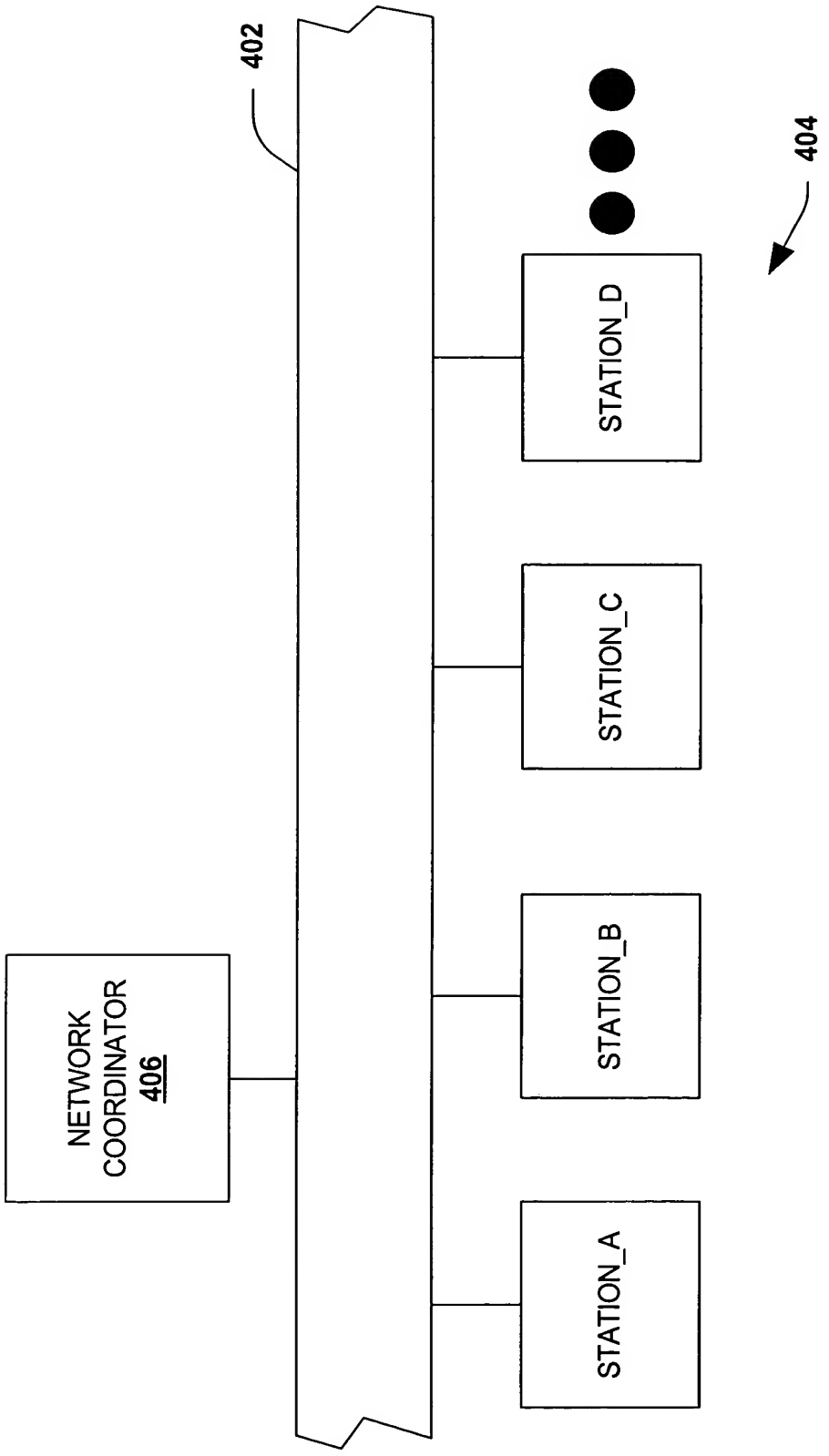
402
404
NETWORK COORDINATOR 406
STATION_A
STATION_B
STATION_C
STATION_D
400

FIG. 4

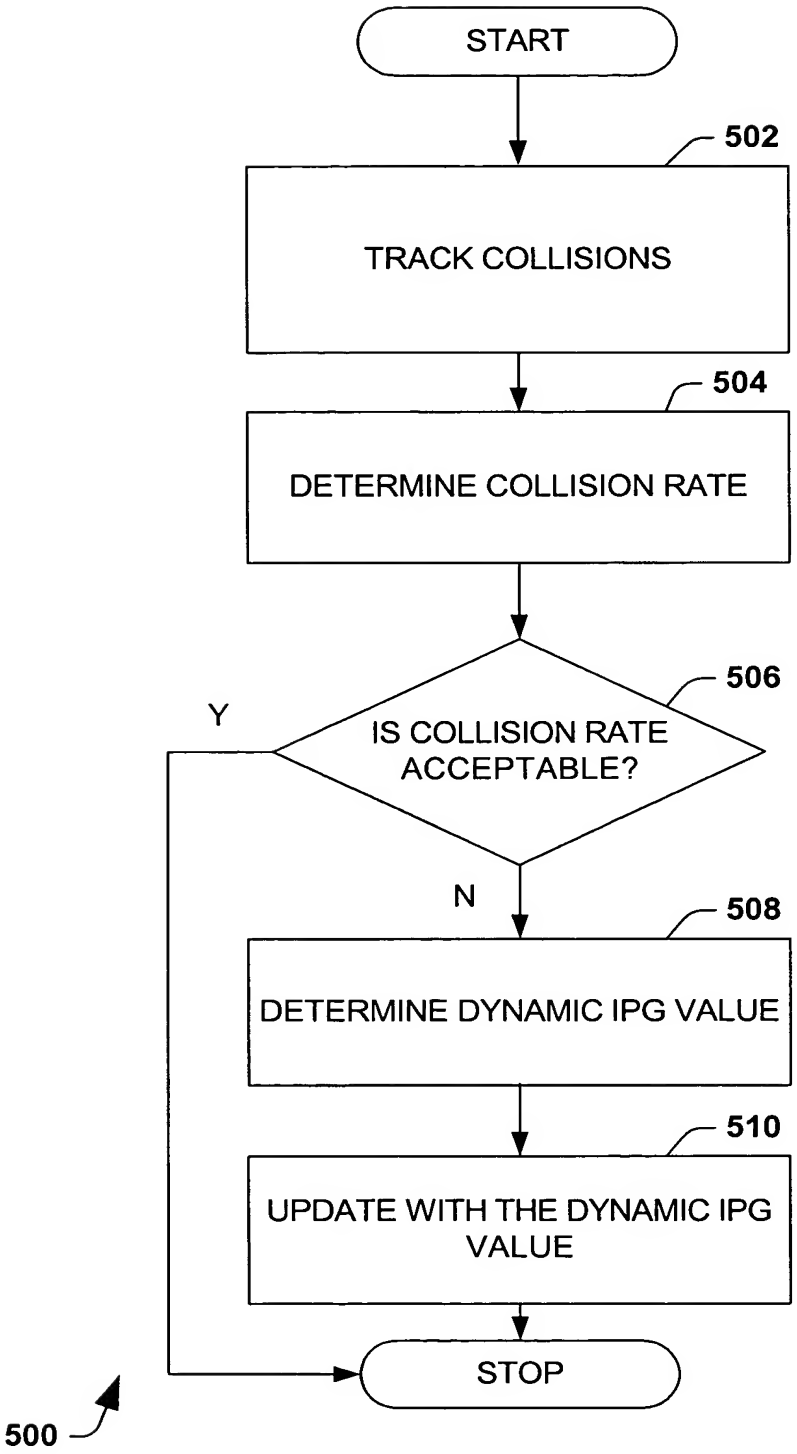
START
502
TRACK COLLISIONS
504
DETERMINE COLLISION RATE
506
IS COLLISION RATE ACCEPTABLE?
Y
N
508
DETERMINE DYNAMIC IPG VALUE
510
UPDATE WITH THE DYNAMIC IPG VALUE
STOP
500

FIG. 5

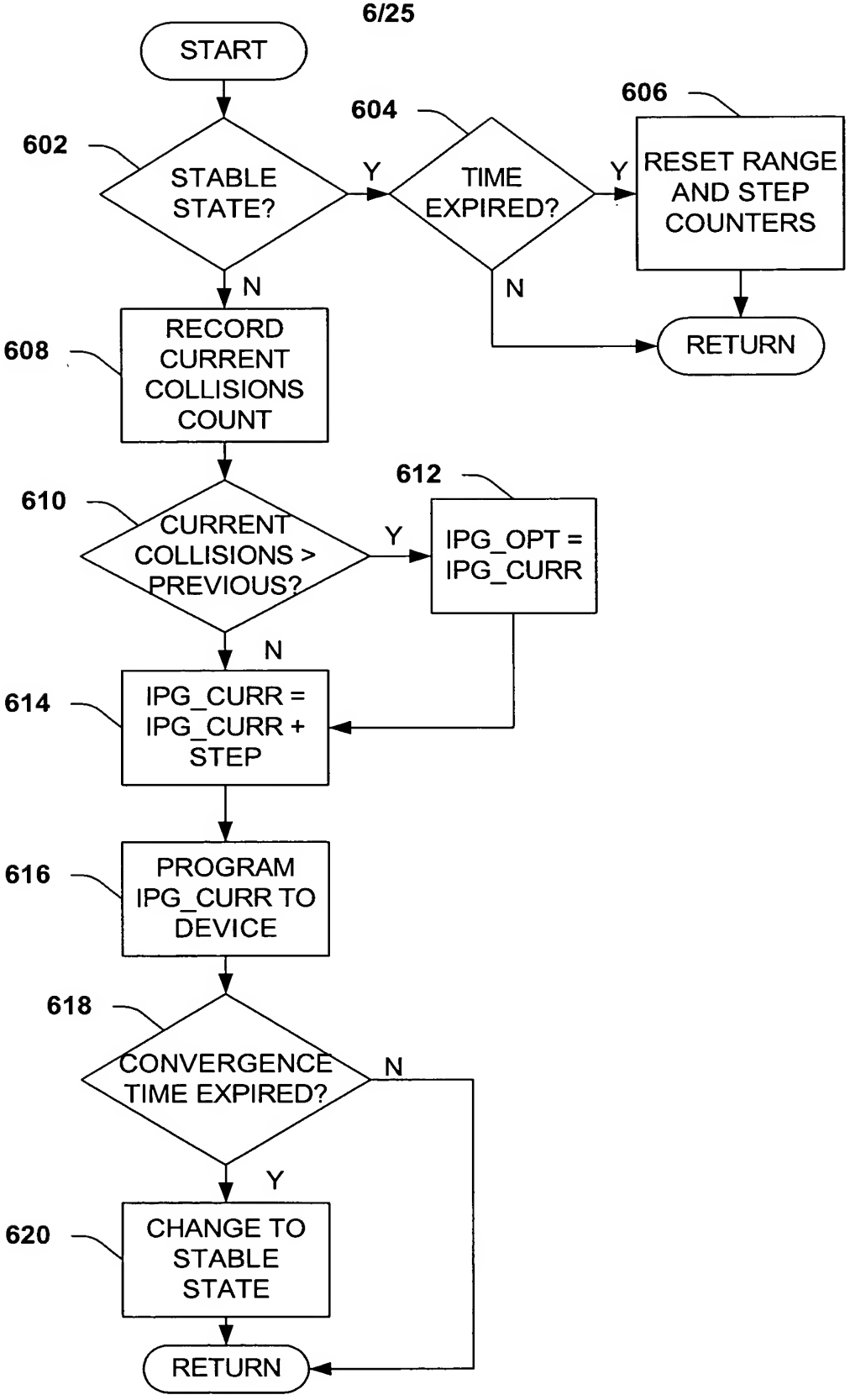
START
602
STABLE STATE?
Y
604
TIME EXPIRED?
Y
606
RESET RANGE AND STEP COUNTERS
N
RETURN
N
608
RECORD CURRENT COLLISIONS COUNT
610
CURRENT COLLISIONS > PREVIOUS?
Y
612
IPG_OPT = IPG_CURR
N
614
IPG_CURR = IPG_CURR + STEP
616
PROGRAM IPG_CURR TO DEVICE
618
CONVERGENCE TIME EXPIRED?
N
Y
620
CHANGE TO STABLE STATE
RETURN
600

FIG. 6

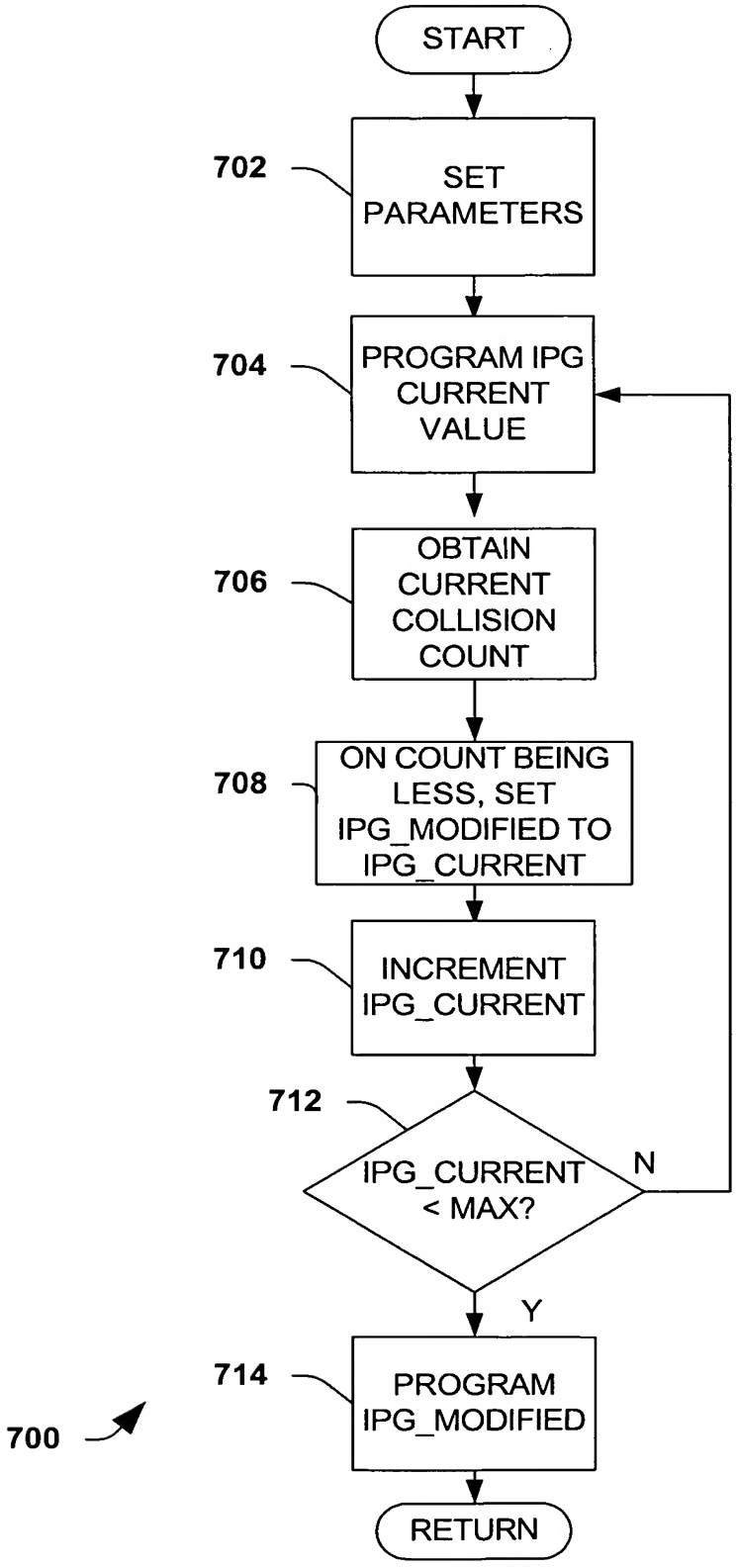
START
702
SET PARAMETERS
704
PROGRAM IPG CURRENT VALUE
706
OBTAIN CURRENT COLLISION COUNT
708
ON COUNT BEING LESS, SET IPG_MODIFIED TO IPG_CURRENT
710
INCREMENT IPG_CURRENT
712
IPG_CURRENT < MAX?
N
Y
714
PROGRAM IPG_MODIFIED
RETURN
700

FIG. 7

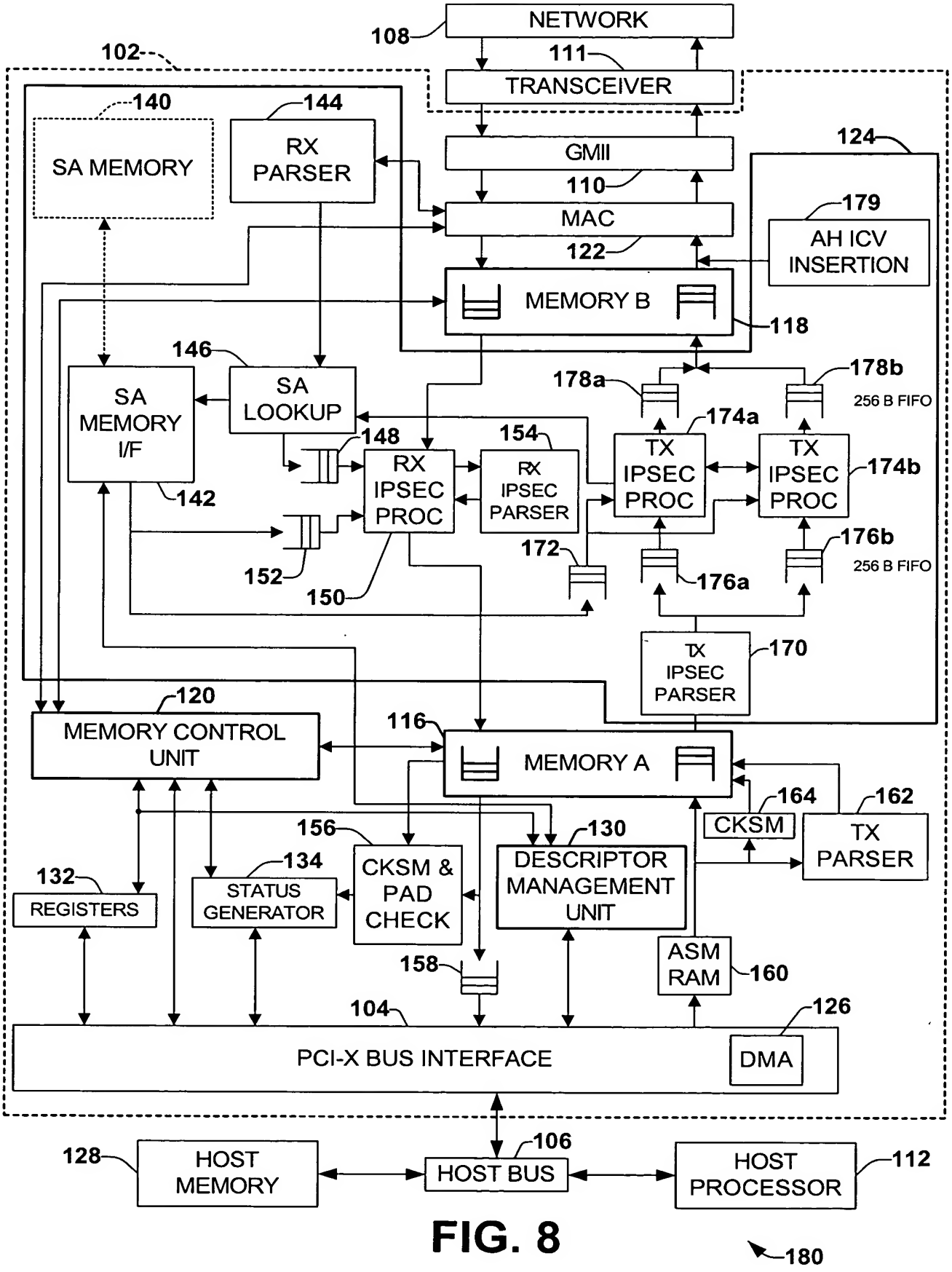
NETWORK
108
111
TRANSCEIVER
102
140
SA MEMORY
144
RX PARSER
GMII
110
124
MAC
122
179
AH ICV INSERTION
MEMORY B
118
146
SA LOOKUP
SA MEMORY I/F
142
178a
178b
256 B FIFO
174a
148
154
RX IPSEC PROC
RX IPSEC PARSER
TX IPSEC PROC
174b
152
150
172
176b
256 B FIFO
176a
TX IPSEC PARSER
170
120
MEMORY CONTROL UNIT
116
MEMORY A
164
162
CKSM
TX PARSER
156
130
134
132
CKSM & PAD CHECK
DESCRIPTOR MANAGEMENT UNIT
REGISTERS
STATUS GENERATOR
158
ASM RAM
160
104
126
PCI-X BUS INTERFACE
DMA
128
HOST MEMORY
106
HOST BUS
HOST PROCESSOR
112
180

FIG. 8

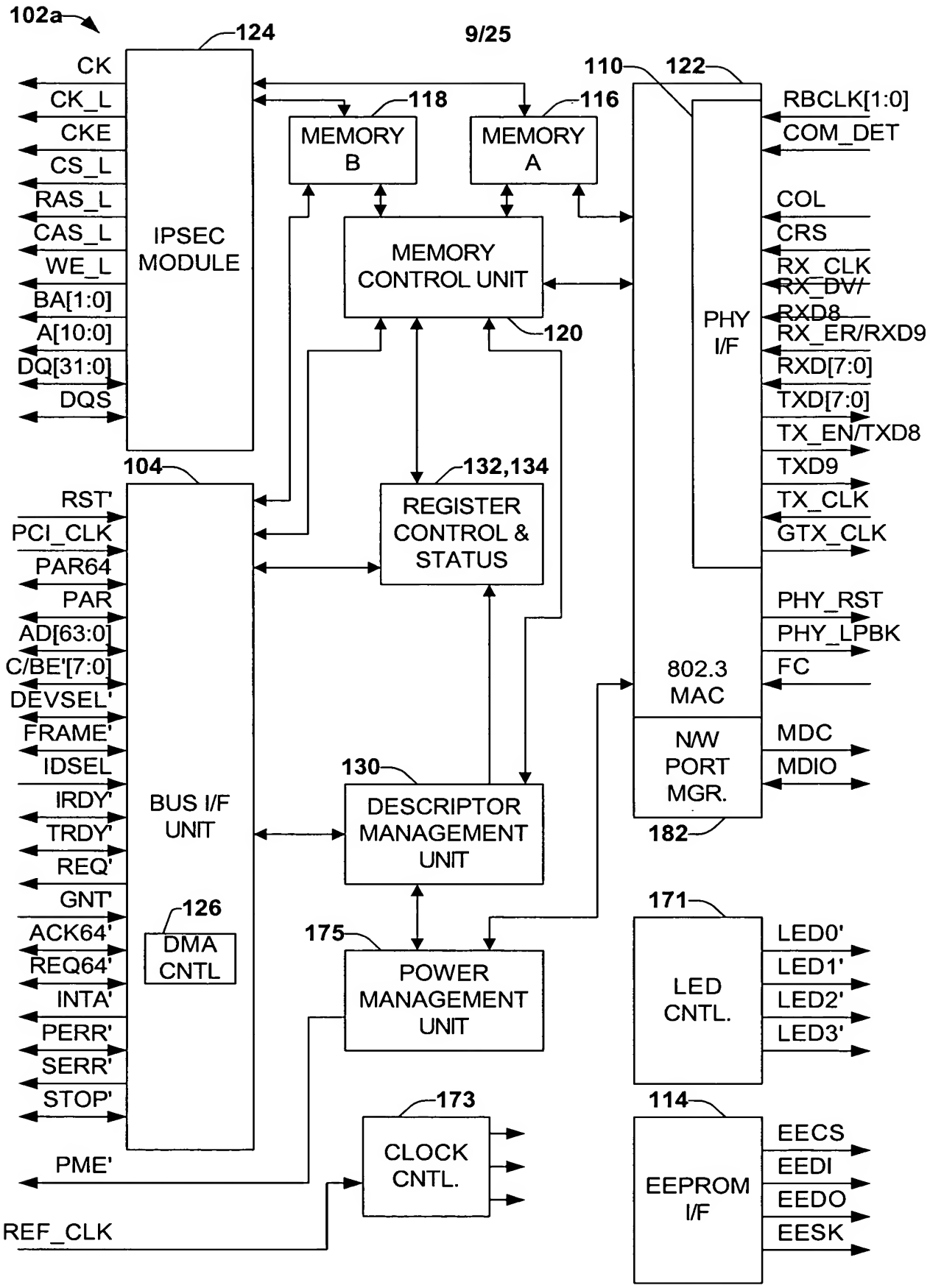
102a
124
CK
CK_L
CKE
CS_L
RAS_L
CAS_L
WE_L
BA[1:0]
A[10:0]
DQ[31:0]
DQS
IPSEC MODULE
118
MEMORY B
116
MEMORY A
MEMORY CONTROL UNIT
120
110
122
PHY I/F
RBCLK[1:0]
COM_DET
COL
CRS
RX_CLK
RX_DV/RXD8
RX_ER/RXD9
RXD[7:0]
TXD[7:0]
TX_EN/TXD8
TXD9
TX_CLK
GTX_CLK
104
132,134
REGISTER CONTROL & STATUS
RST'
PCI_CLK
PAR64
PAR
AD[63:0]
C/BE'[7:0]
DEVSEL'
FRAME'
IDSEL
IRDY'
TRDY'
REQ'
GNT'
ACK64'
REQ64'
INTA'
PERR'
SERR'
STOP'
BUS I/F UNIT
126
DMA CNTL
130
DESCRIPTOR MANAGEMENT UNIT
175
POWER MANAGEMENT UNIT
802.3 MAC
N/W PORT MGR.
182
PHY_RST
PHY_LPBK
FC
MDC
MDIO
171
LED CNTL.
LED0'
LED1'
LED2'
LED3'
173
CLOCK CNTL.
PME'
REF_CLK
114
EEPROM I/F
EECS
EEDI
EEDO
EESK

FIG. 9

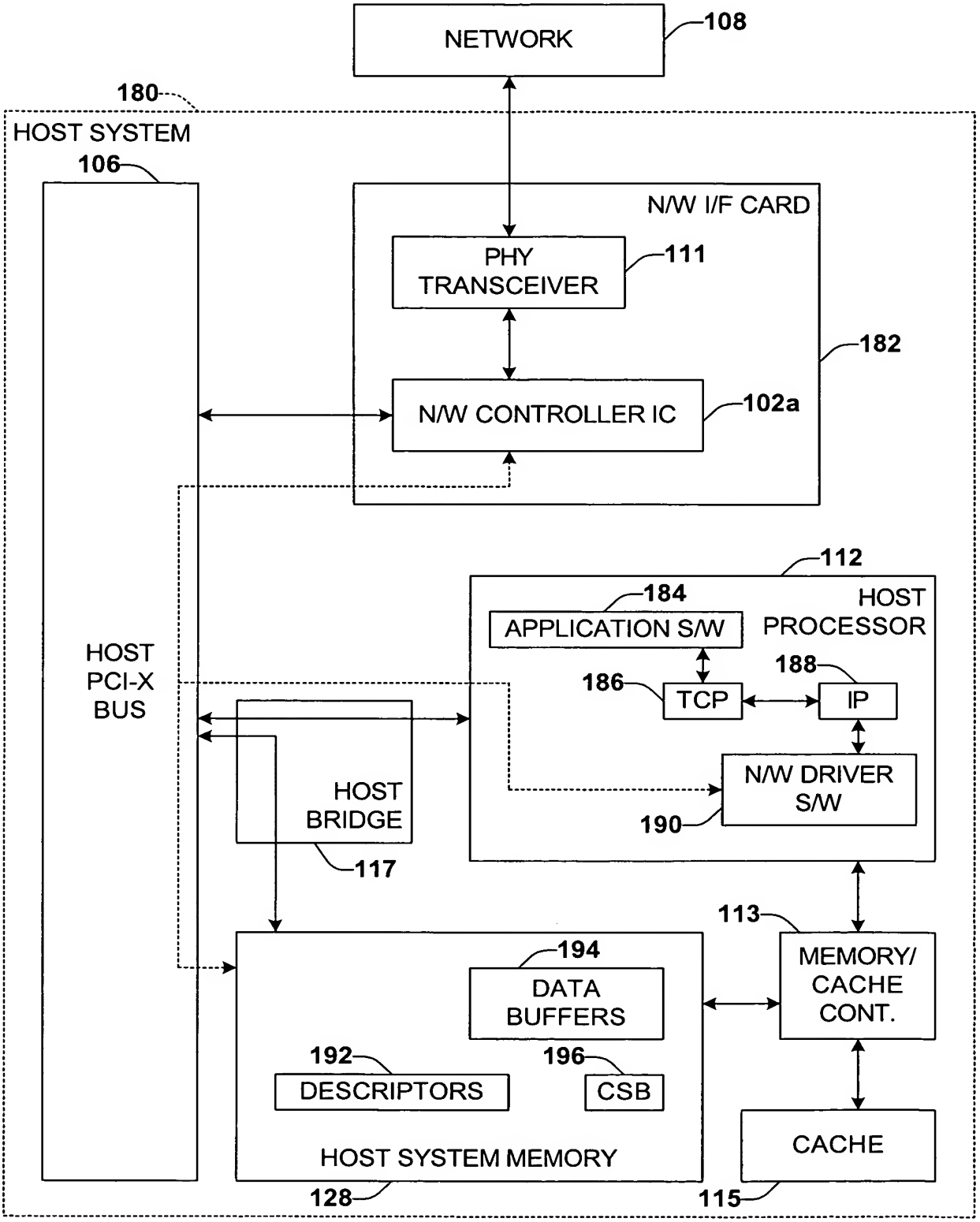
NETWORK
108
180
HOST SYSTEM
106
N/W I/F CARD
PHY TRANSCEIVER
111
182
N/W CONTROLLER IC
102a
112
184
APPLICATION S/W
HOST PROCESSOR
188
186
TCP
IP
HOST PCI-X BUS
N/W DRIVER S/W
190
HOST BRIDGE
117
113
194
DATA BUFFERS
MEMORY/ CACHE CONT.
192
196
DESCRIPTORS
CSB
HOST SYSTEM MEMORY
CACHE
128
115

FIG. 10

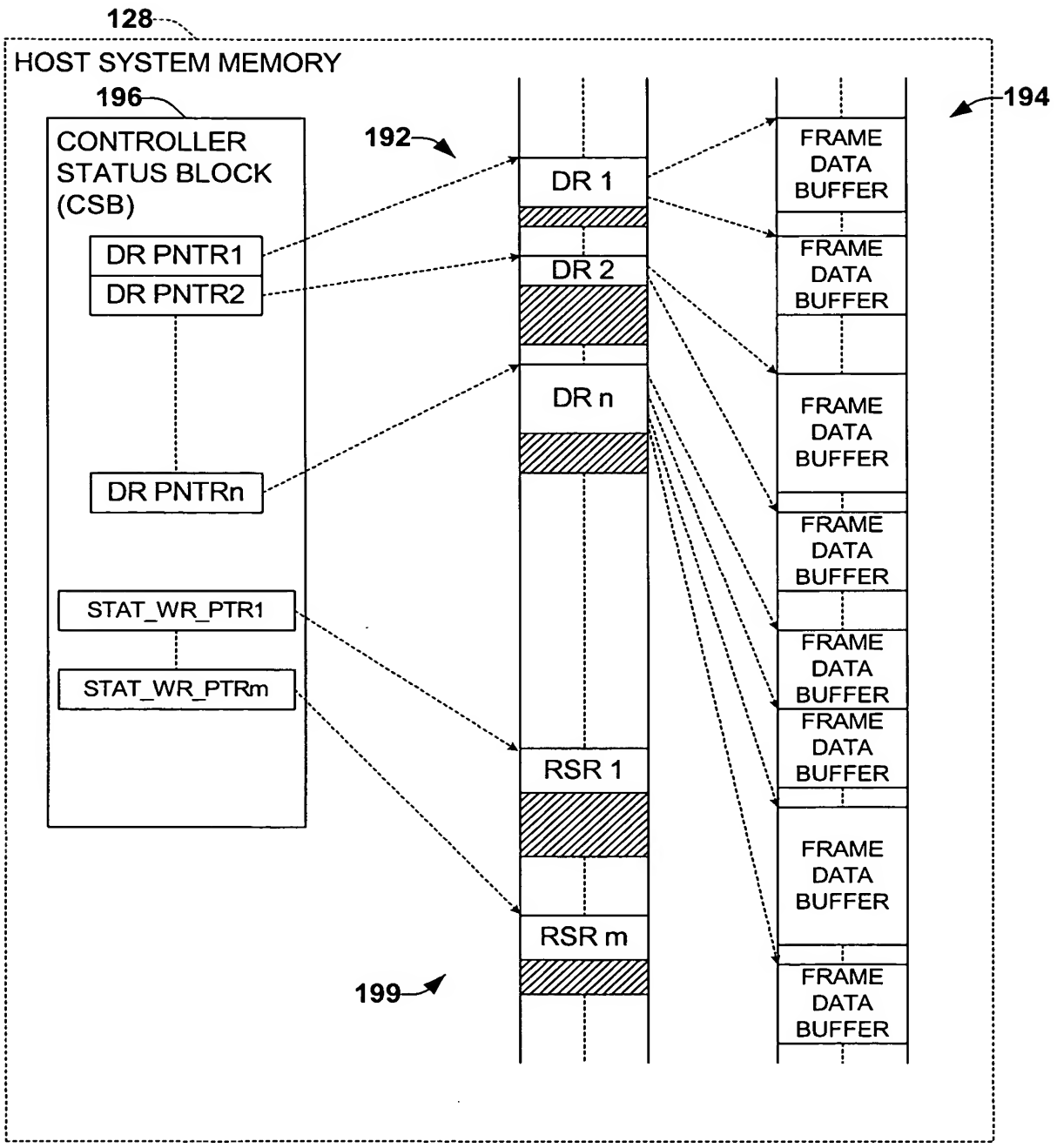
128
HOST SYSTEM MEMORY
196
CONTROLLER STATUS BLOCK (CSB)
DR PNTR1
DR PNTR2
DR PNTRn
STAT_WR_PTR1
STAT_WR_PTRm
192
DR 1
DR 2
DR n
RSR 1
RSR m
199
194
FRAME DATA BUFFER
FRAME DATA BUFFER
FRAME DATA BUFFER
FRAME DATA BUFFER
FRAME DATA BUFFER
FRAME DATA BUFFER
FRAME DATA BUFFER
FRAME DATA BUFFER

FIG. 11A

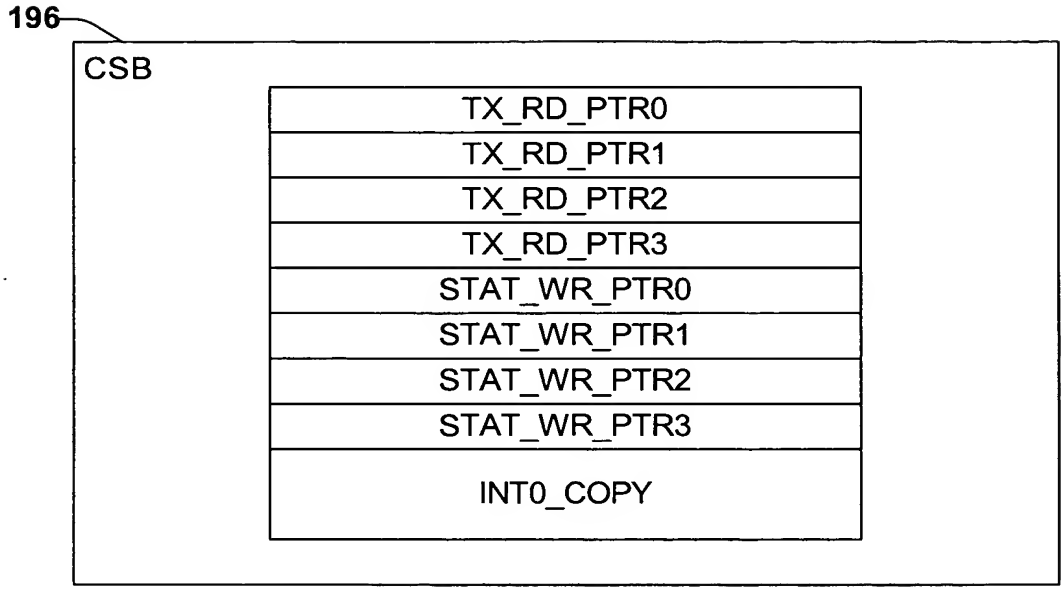

FIG. 11B

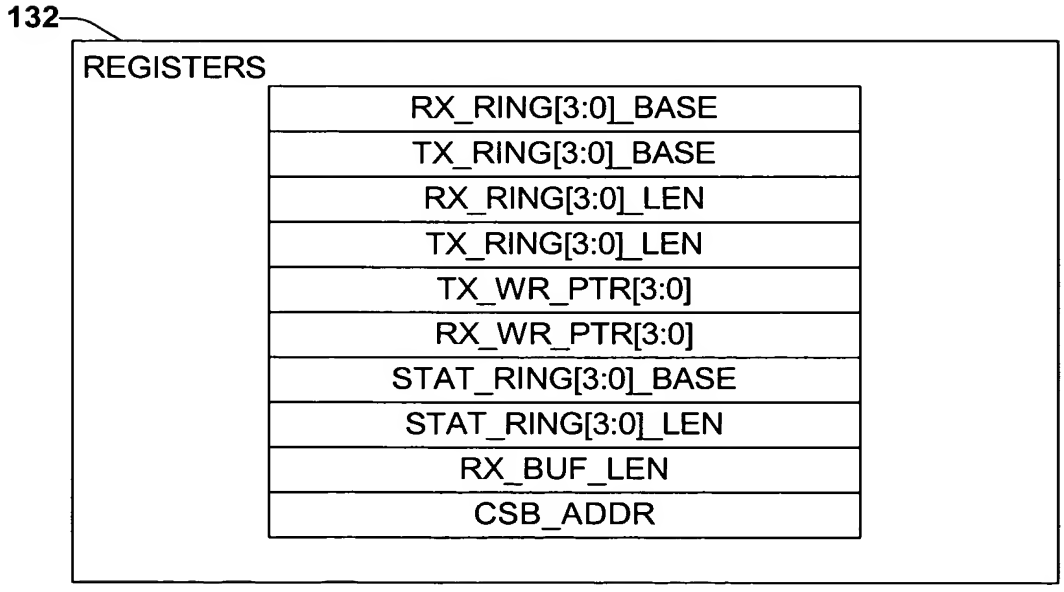

FIG. 11C

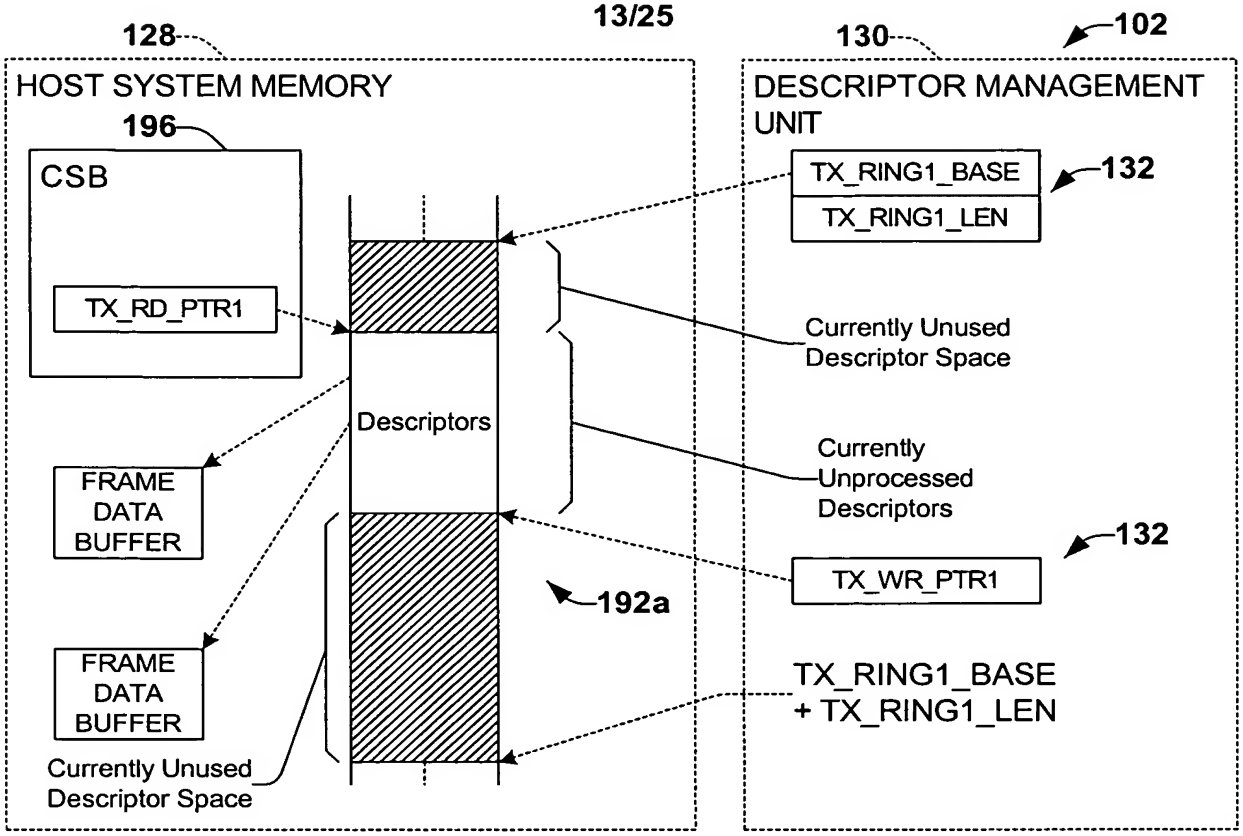

FIG. 11D

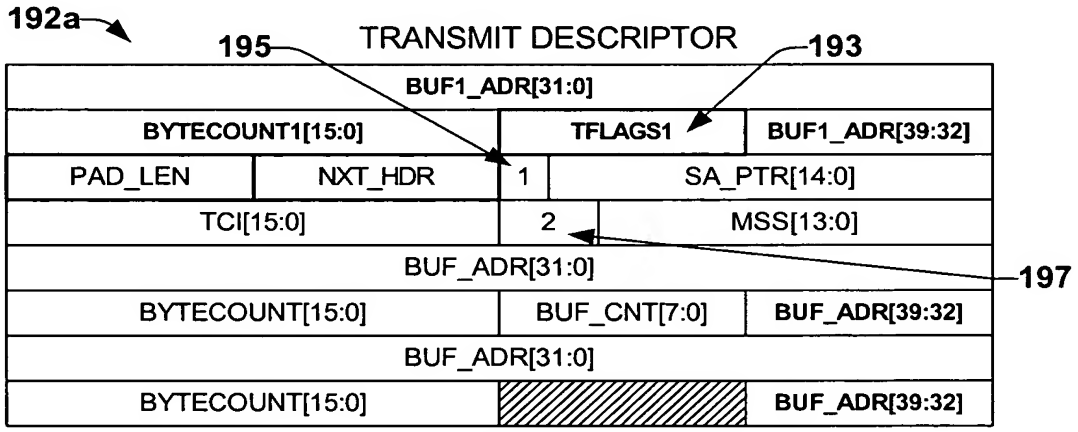

FIG. 11E

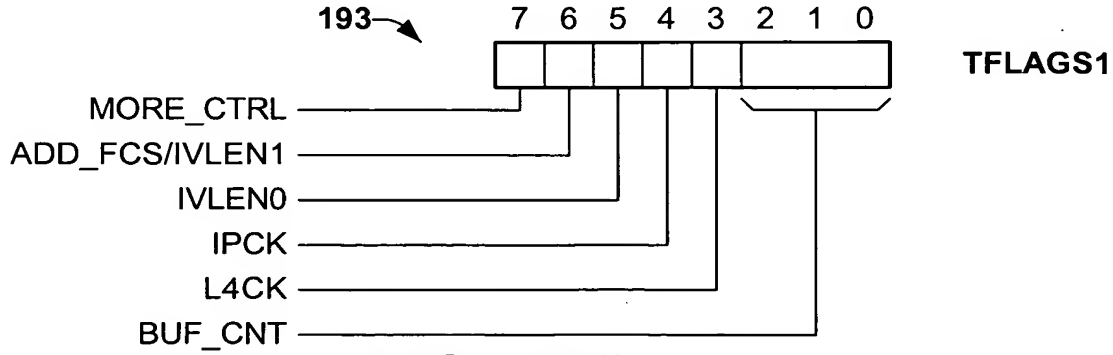

FIG. 11F

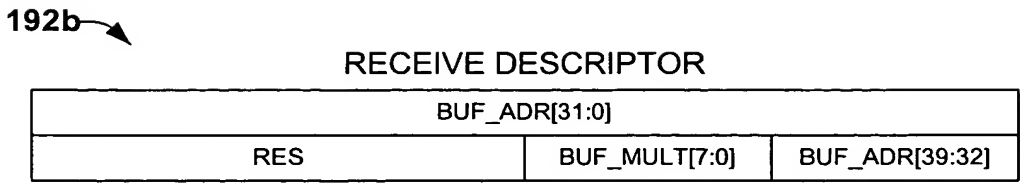

FIG. 11G

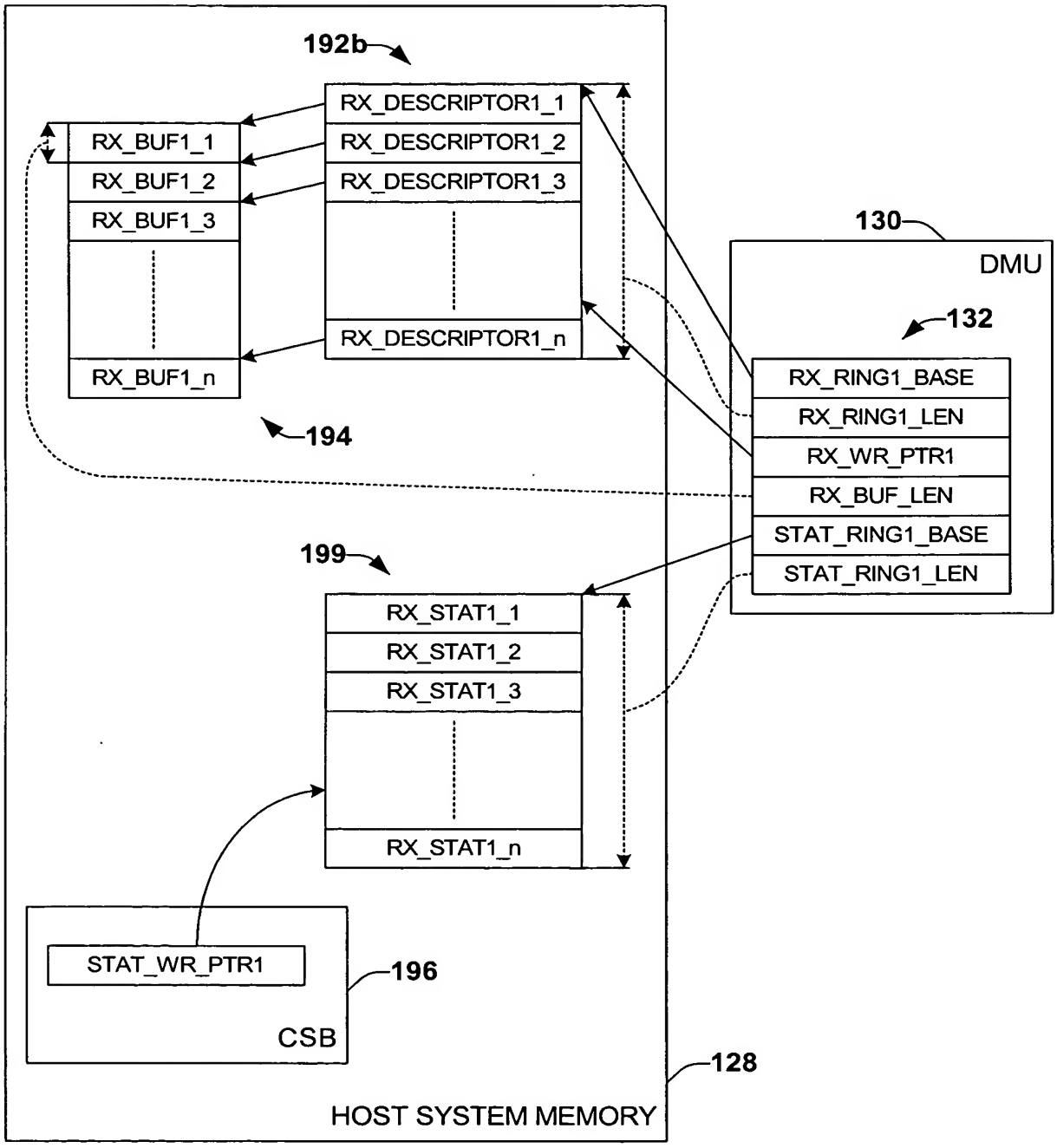

FIG. 11H

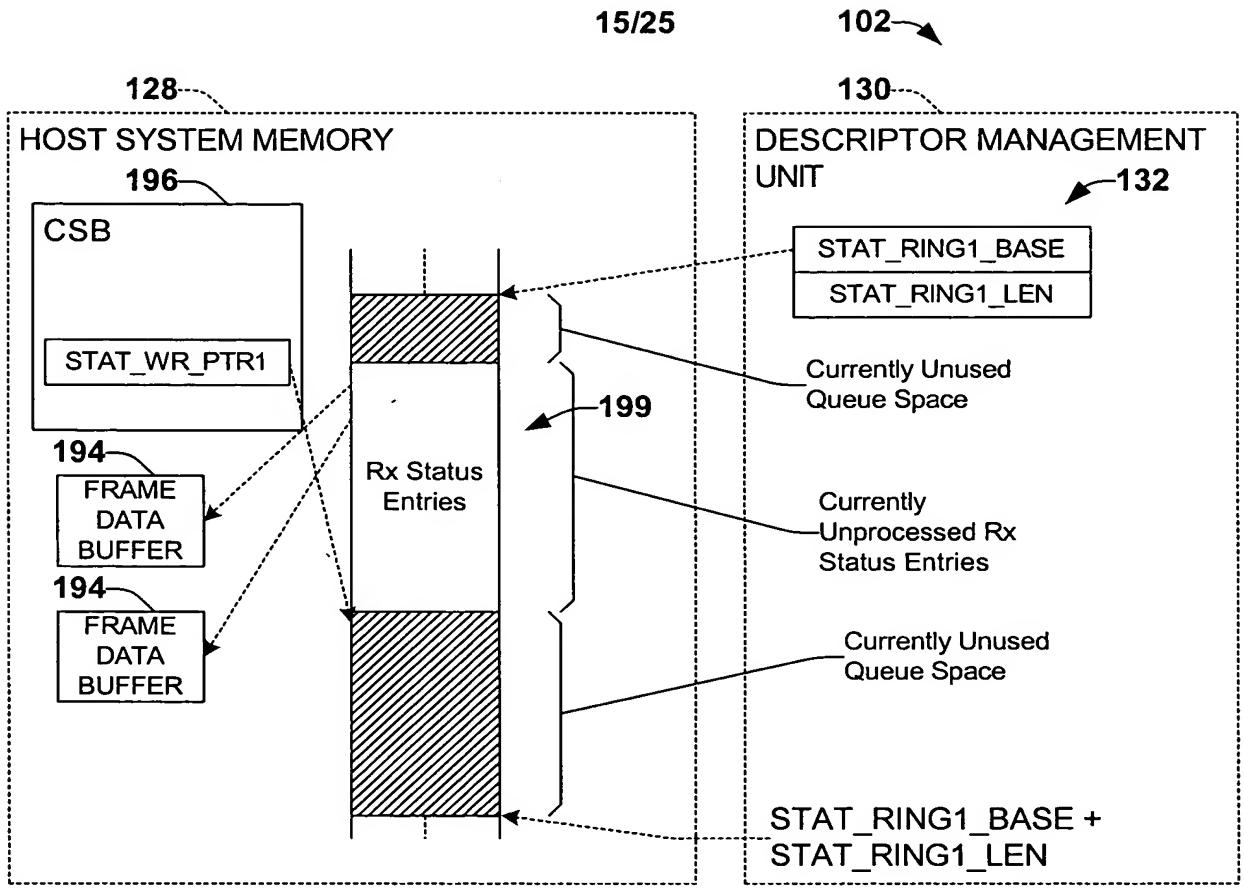

FIG. 11I

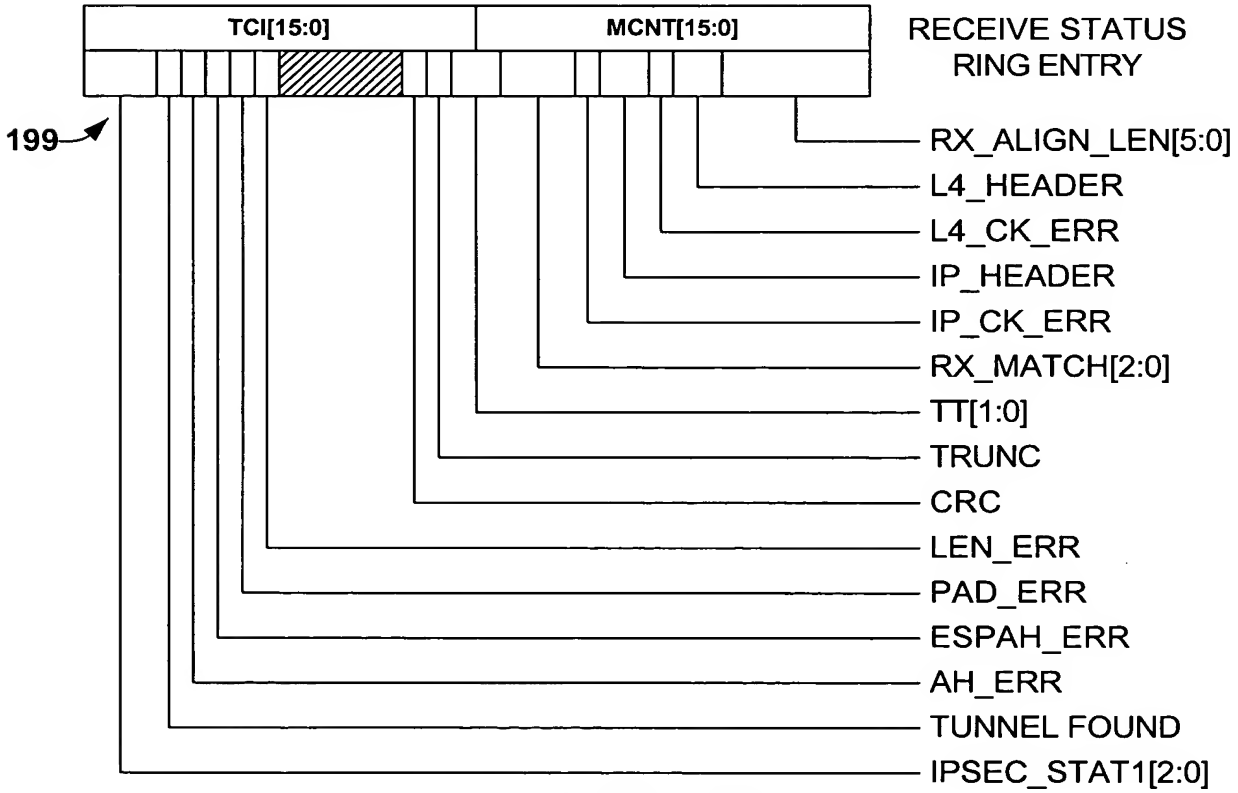

FIG. 11J

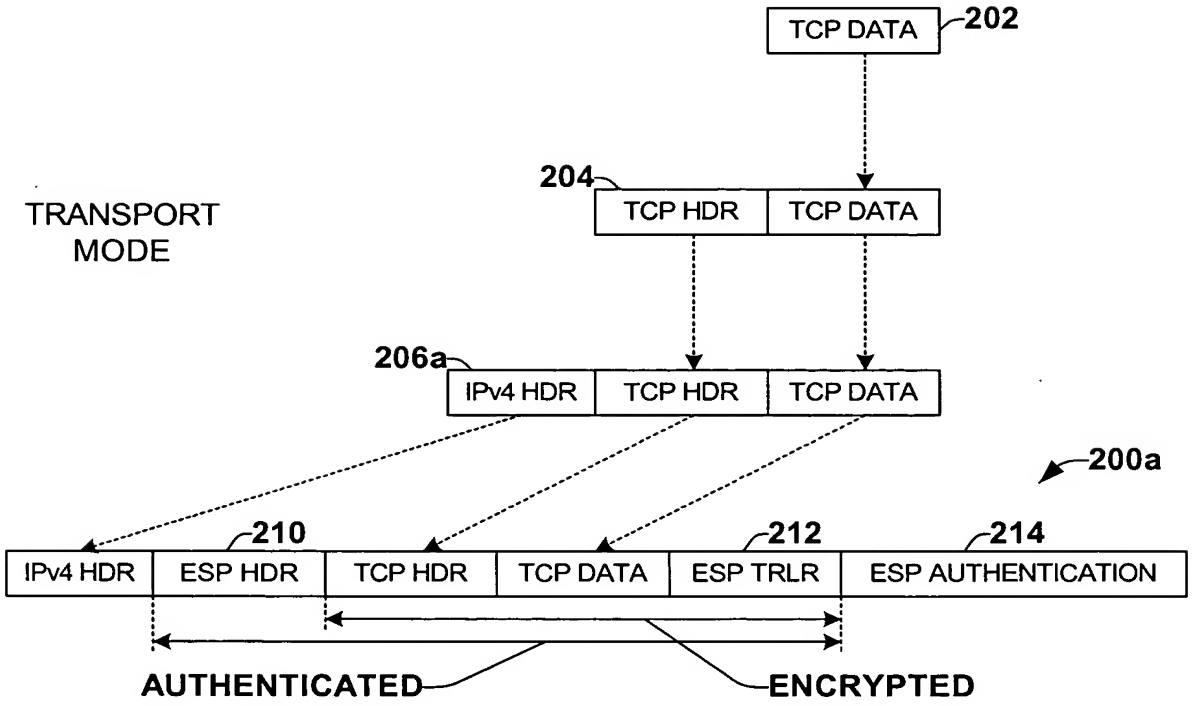

FIG. 12A

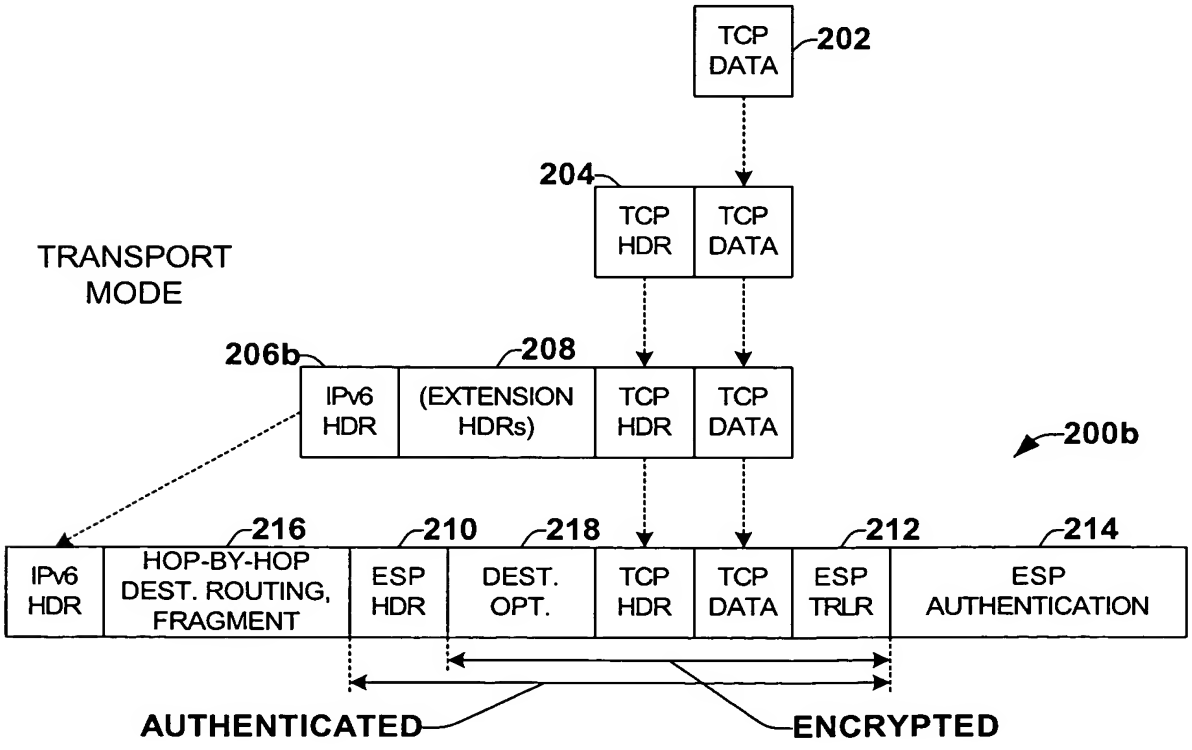

FIG. 12B

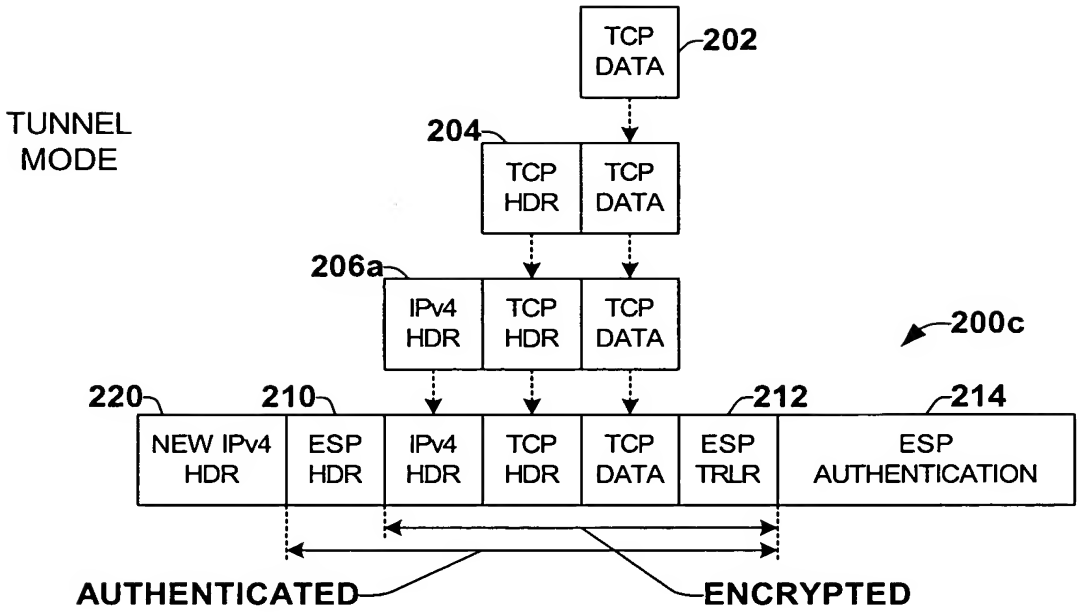

FIG. 12C

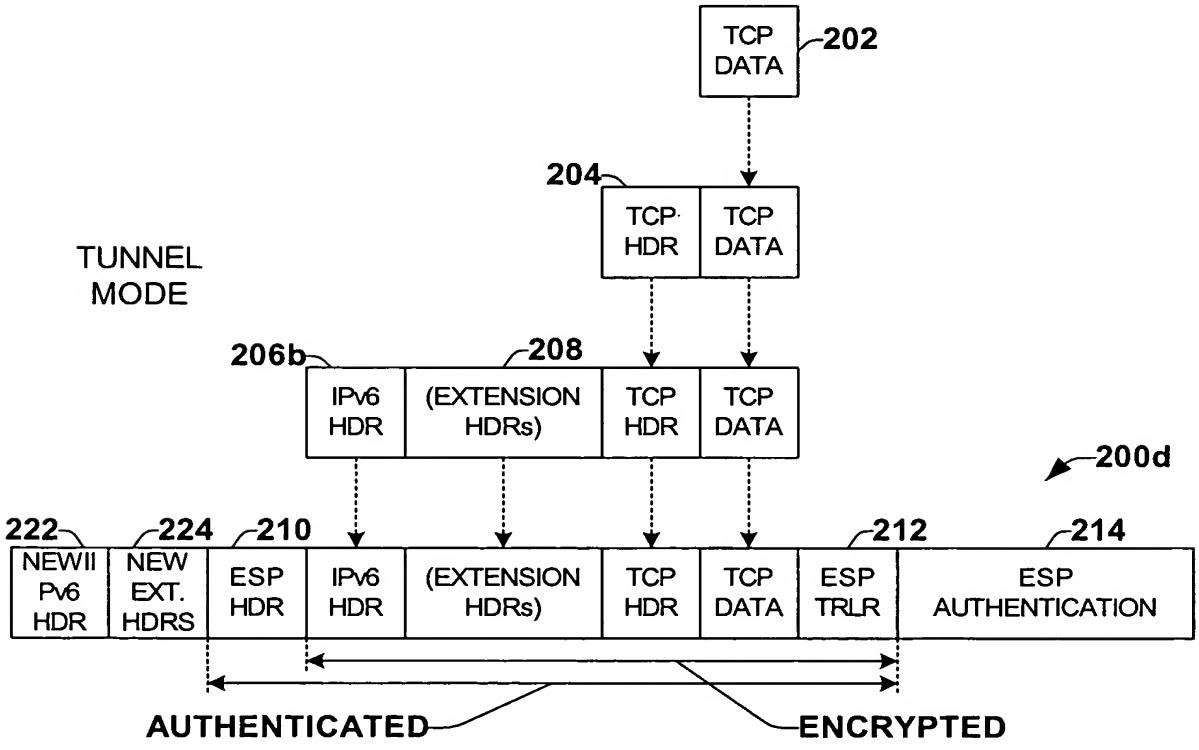

FIG. 12D

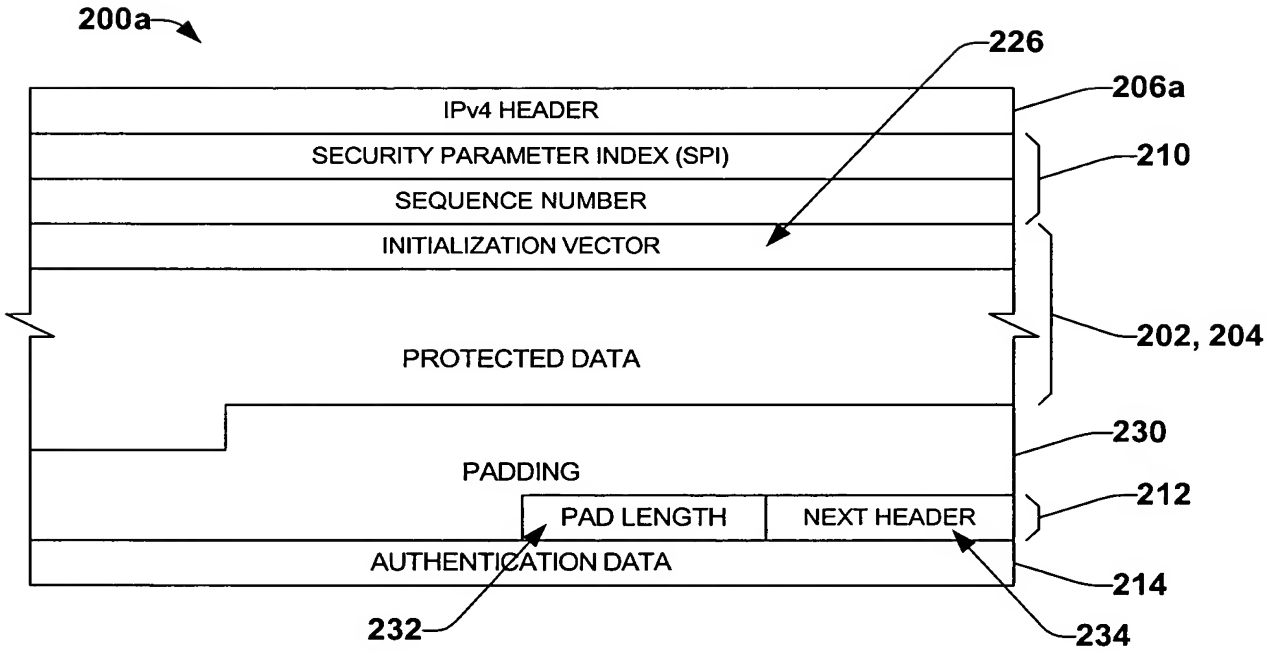
200a
226
206a
IPv4 HEADER
SECURITY PARAMETER INDEX (SPI)
SEQUENCE NUMBER
INITIALIZATION VECTOR
210
PROTECTED DATA
202, 204
230
PADDING
PAD LENGTH
NEXT HEADER
212
AUTHENTICATION DATA
214
232
234

FIG. 12E

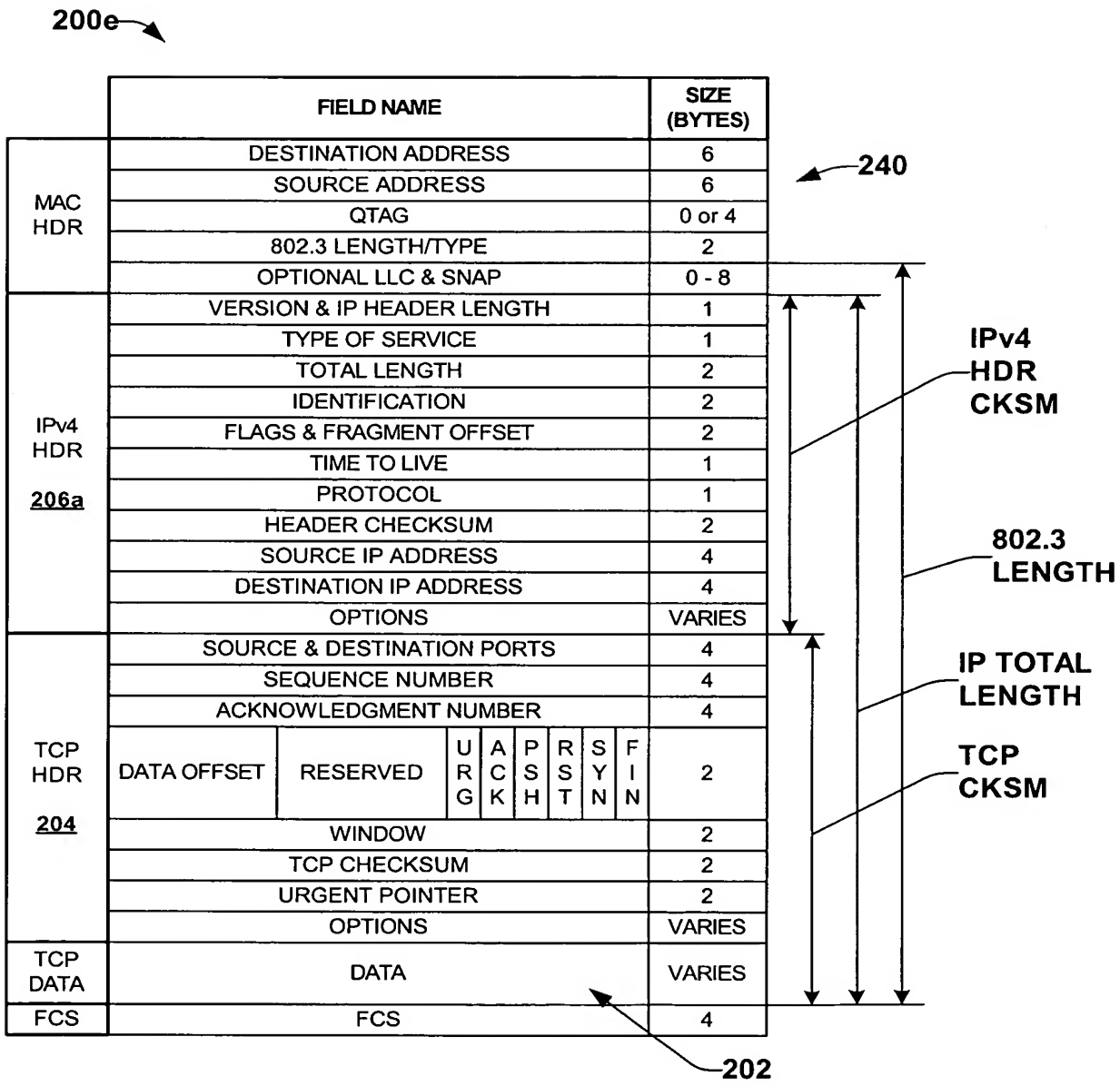
200e
FIELD NAME
SIZE (BYTES)
MAC HDR
DESTINATION ADDRESS 6
SOURCE ADDRESS 6
QTAG 0 or 4
802.3 LENGTH/TYPE 2
OPTIONAL LLC & SNAP 0 - 8
IPv4 HDR 206a
VERSION & IP HEADER LENGTH 1
TYPE OF SERVICE 1
TOTAL LENGTH 2
IDENTIFICATION 2
FLAGS & FRAGMENT OFFSET 2
TIME TO LIVE 1
PROTOCOL 1
HEADER CHECKSUM 2
SOURCE IP ADDRESS 4
DESTINATION IP ADDRESS 4
OPTIONS VARIES
TCP HDR 204
SOURCE & DESTINATION PORTS 4
SEQUENCE NUMBER 4
ACKNOWLEDGMENT NUMBER 4
DATA OFFSET
RESERVED
URG ACK PSH RST SYN FIN
2
WINDOW 2
TCP CHECKSUM 2
URGENT POINTER 2
OPTIONS VARIES
TCP DATA
DATA VARIES
FCS
FCS 4
240
IPv4 HDR CKSM
802.3 LENGTH
IP TOTAL LENGTH
TCP CKSM
202

FIG. 13A

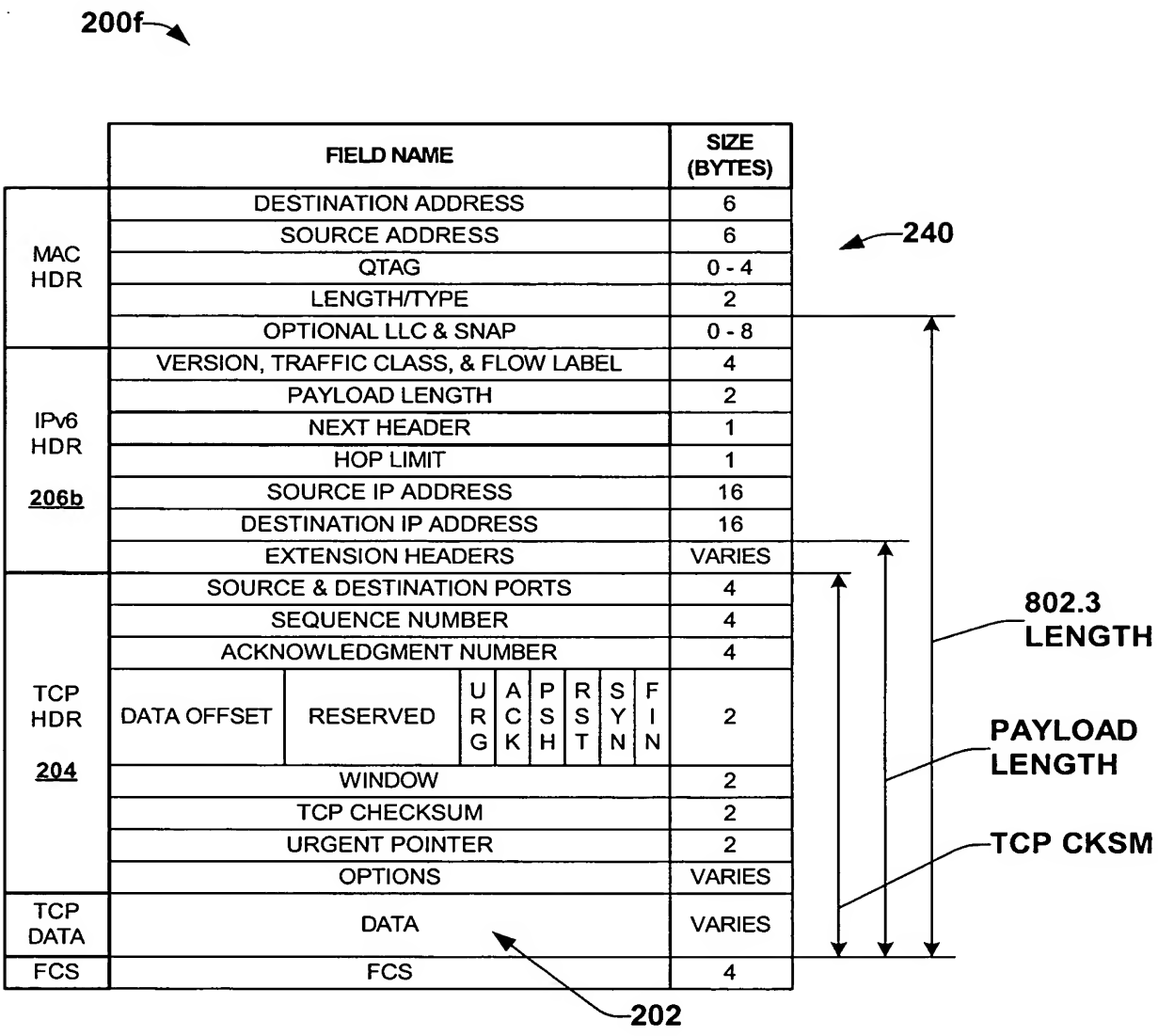
200f
FIELD NAME
SIZE (BYTES)
MAC HDR
DESTINATION ADDRESS 6
SOURCE ADDRESS 6
QTAG 0 - 4
LENGTH/TYPE 2
OPTIONAL LLC & SNAP 0 - 8
IPv6 HDR
206b
VERSION, TRAFFIC CLASS, & FLOW LABEL 4
PAYLOAD LENGTH 2
NEXT HEADER 1
HOP LIMIT 1
SOURCE IP ADDRESS 16
DESTINATION IP ADDRESS 16
EXTENSION HEADERS VARIES
TCP HDR
204
SOURCE & DESTINATION PORTS 4
SEQUENCE NUMBER 4
ACKNOWLEDGMENT NUMBER 4
DATA OFFSET
RESERVED
URG
ACK
PSH
RST
SYN
FIN
2
WINDOW 2
TCP CHECKSUM 2
URGENT POINTER 2
OPTIONS VARIES
TCP DATA
DATA VARIES
FCS
FCS 4
240
802.3 LENGTH
PAYLOAD LENGTH
TCP CKSM
202

FIG. 13B

250

FIELD NAME	Created by Host	Modified by ESP	Encrypted	Covered by ESP Authentication	Added by Controller
Preamble					x
Start of Frame Delimiter					x
MAC Header	x				
IP Header	x				
ESP Header	x			x	
Payload Data	x	x	x	x	
Padding	x	x	x	x	
Pad Length	x	x	x	x	
Next Header	x	x	x	x	
Authentication Data	x	x			
Frame Check Sequence					x

FIG. 14A

252

FIELD NAME	Created by Host	Modified by AH Module	Covered by AH Authentication	Added by Controller
Preamble				x
Start of Frame Delimiter				x
MAC Header	x			
IP Header	x		x	
AH Header	x	x	x	
Other Headers	x		x	
Payload Data	x		x	
Frame Check Sequence				X

FIG. 14B

254

PHCKSM FOR IPv4	
32-BIT IP SOURCE ADDRESS	
32-BIT IP DESTINATION ADDRESS	
ZERO	PROTOCOL
TCP TOTAL LENGTH	

FIG. 14C

256

PHCKSM FOR IPv6	
128-BIT IP SOURCE ADDRESS	
128-BIT IP DESTINATION ADDRESS	
16-BIT TCP TOTAL LENGTH	
ZERO	PROTOCOL

FIG. 14D

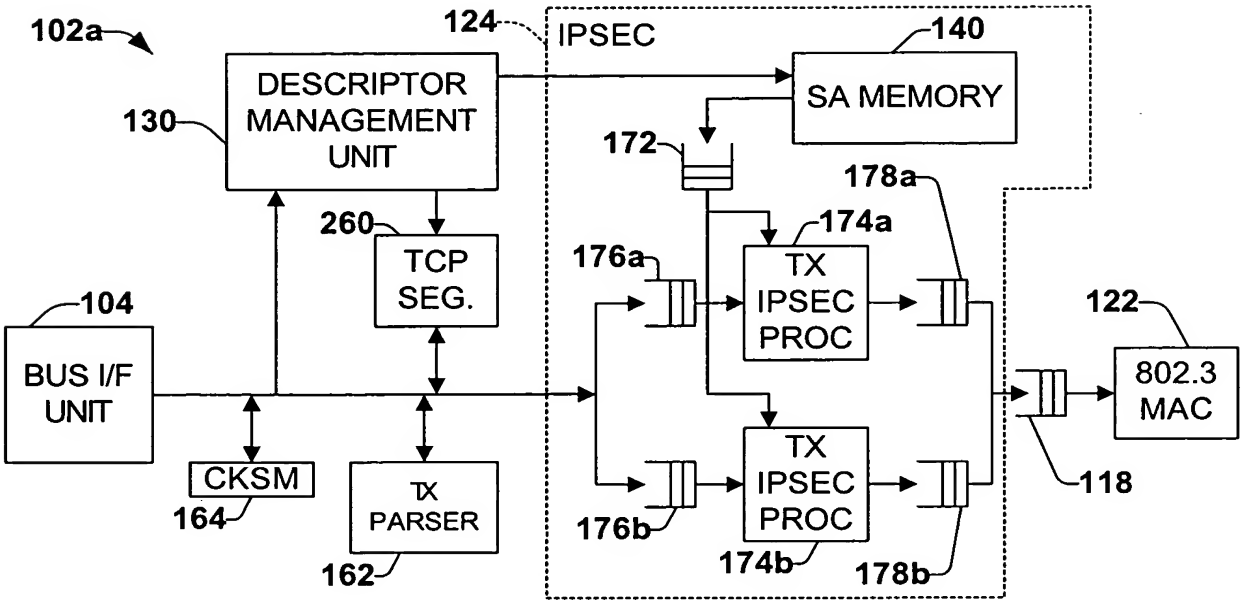
102a
124
IPSEC
140
SA MEMORY
DESCRIPTOR MANAGEMENT UNIT
130
172
178a
260
TCP SEG.
174a
176a
TX IPSEC PROC
104
122
BUS I/F UNIT
802.3 MAC
CKSM
164
TX PARSER
162
TX IPSEC PROC
176b
174b
178b
118

FIG. 15

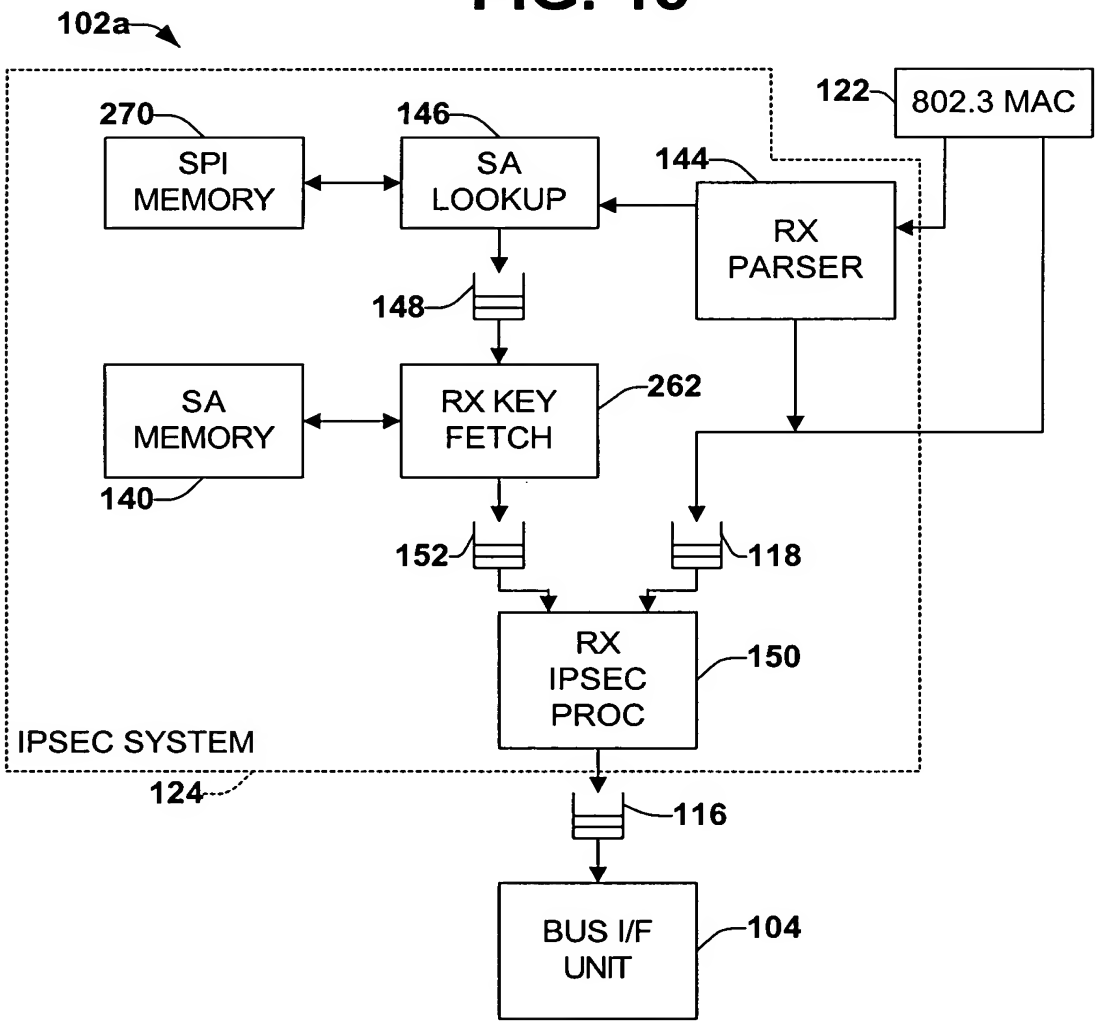
102a
122
802.3 MAC
270
SPI MEMORY
146
SA LOOKUP
144
RX PARSER
148
SA MEMORY
140
RX KEY FETCH
262
152
118
RX IPSEC PROC
150
IPSEC SYSTEM
124
116
BUS I/F UNIT
104

FIG. 16

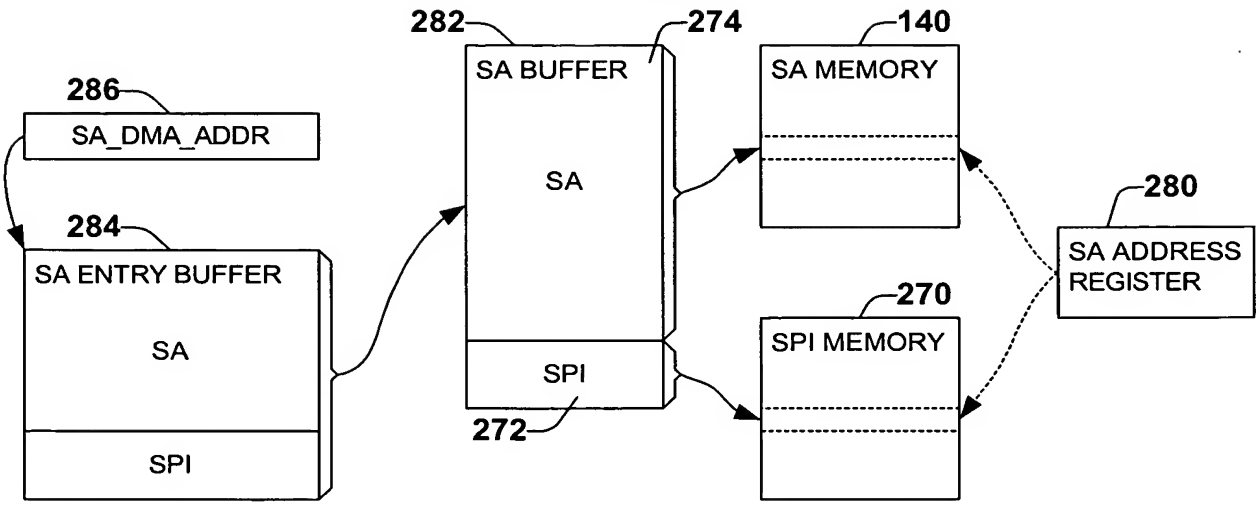

FIG. 17A

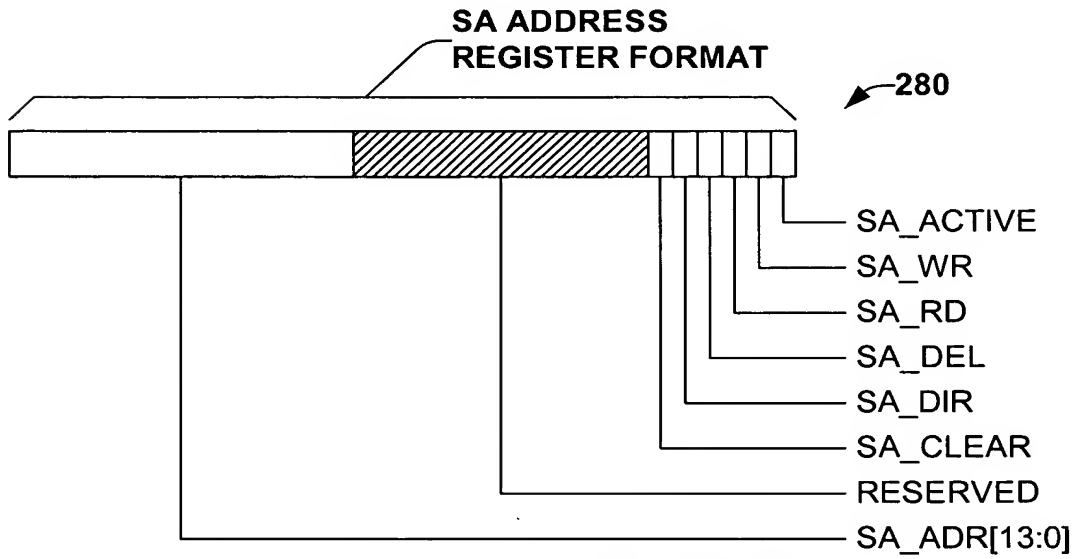

FIG. 17B

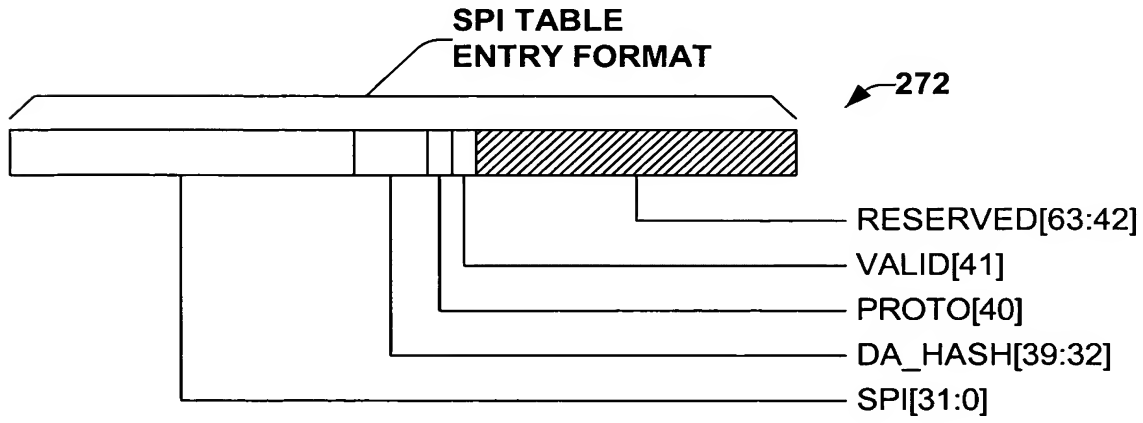

FIG. 17C

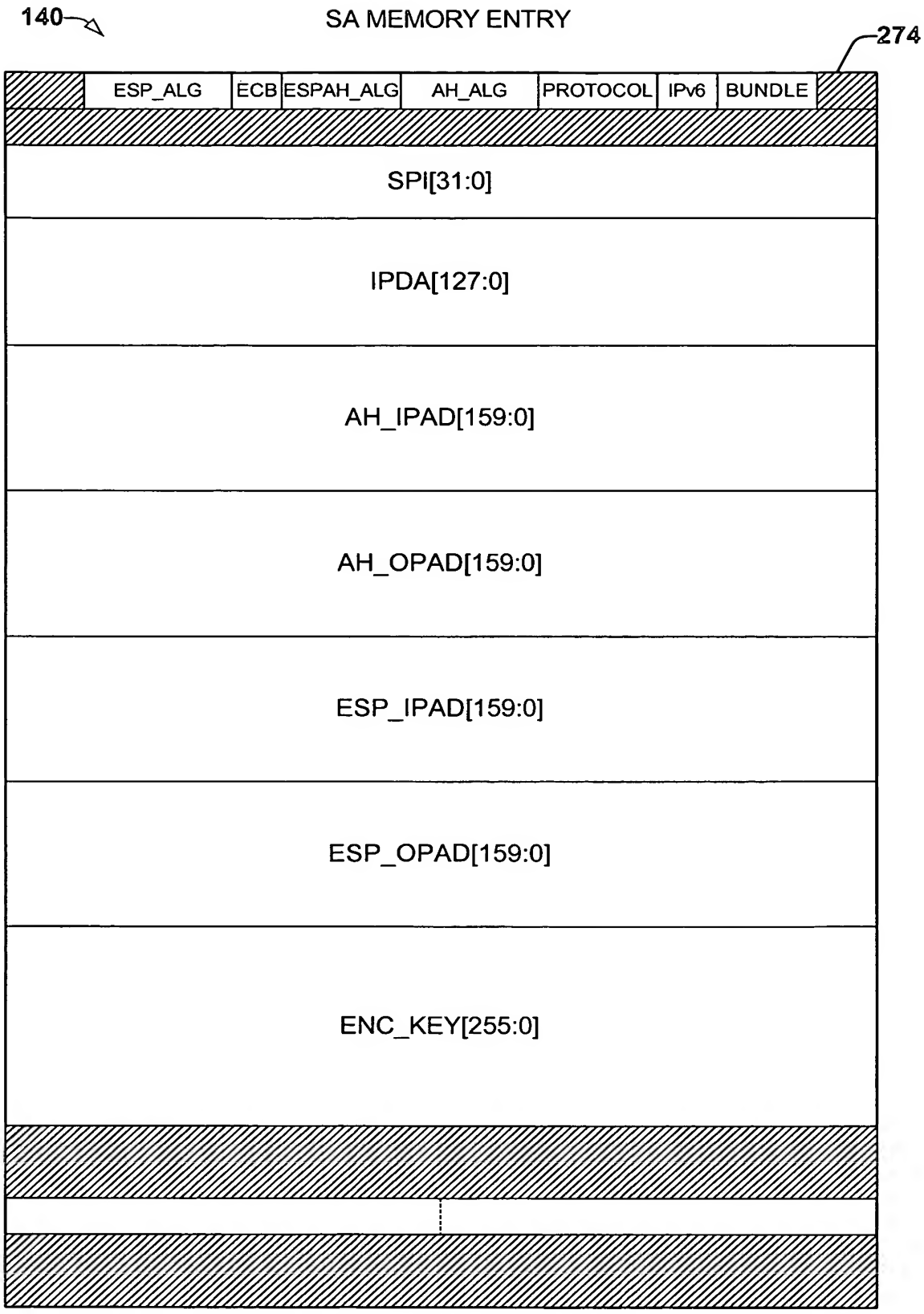
140
SA MEMORY ENTRY
274
ESP_ALG
ECB
ESPAH_ALG
AH_ALG
PROTOCOL
IPv6
BUNDLE
SPI[31:0]
IPDA[127:0]
AH_IPAD[159:0]
AH_OPAD[159:0]
ESP_IPAD[159:0]
ESP_OPAD[159:0]
ENC_KEY[255:0]

FIG. 17D